

32-BIT ARM7TDMI-BASED MCU

NUC501 Development Board User Guide

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32-BIT ARM7TDMI-BASED MCU**Revision history**

version	date	page	description
A	Dec 20, 2008	--	Initial Issued
B	Jan. 06, 2009	--	Add board picture
C	Mar.12, 2009	--	Update
D	Apr.28,2009	--	Update schematic

32-BIT ARM7TDMI-BASED MCU

TABLE OF CONTENTS -

REVISION HISTORY	2
1 INTRODUCTION	4
1.1 THE NUC501 DEVELOPMENT BOARD	5
1.1.1 DEV Board layout and connectors	6
1.2 THE NUC501DN CPU BOARD	13
1.2.1 Board layout and connectors	14
1.3 THE VPP SUPPLIER BOARD	15
1.3.1 Board layout and connectors	15
2 GETTING STARTED	17
2.1 NUC501 I/O PIN FUNCTION.....	18
2.2 JUMPER SETTINGS	20
2.2.1 Power-On Settings	20
2.2.2 GPIO Jumpers	23
3 SCHEMATIC.....	27
4 BOM LIST	39

32-BIT ARM7TDMI-BASED MCU

1 Introduction

The NUC501 DEV is an evaluation board for NUVOTON's ARM7TDMI-based NUC501 series microcontrollers. It provides a complete development environment for NUC501 microcontrollers which has 32KB internal SRAM and boot ROM ,crypto engine with OTP key, build-in 1.8V LDO , supports up to 37 GPIOs, 4-ch PWM, two UART channels , three SPI/Micro-wire channels, one I²C channel and 20-pin JTAG ICE interface for debugging.

The user guide provides information about hardware features and information about using this development board. The picture of NUC501 DEV Board shows on Figure 1-1.

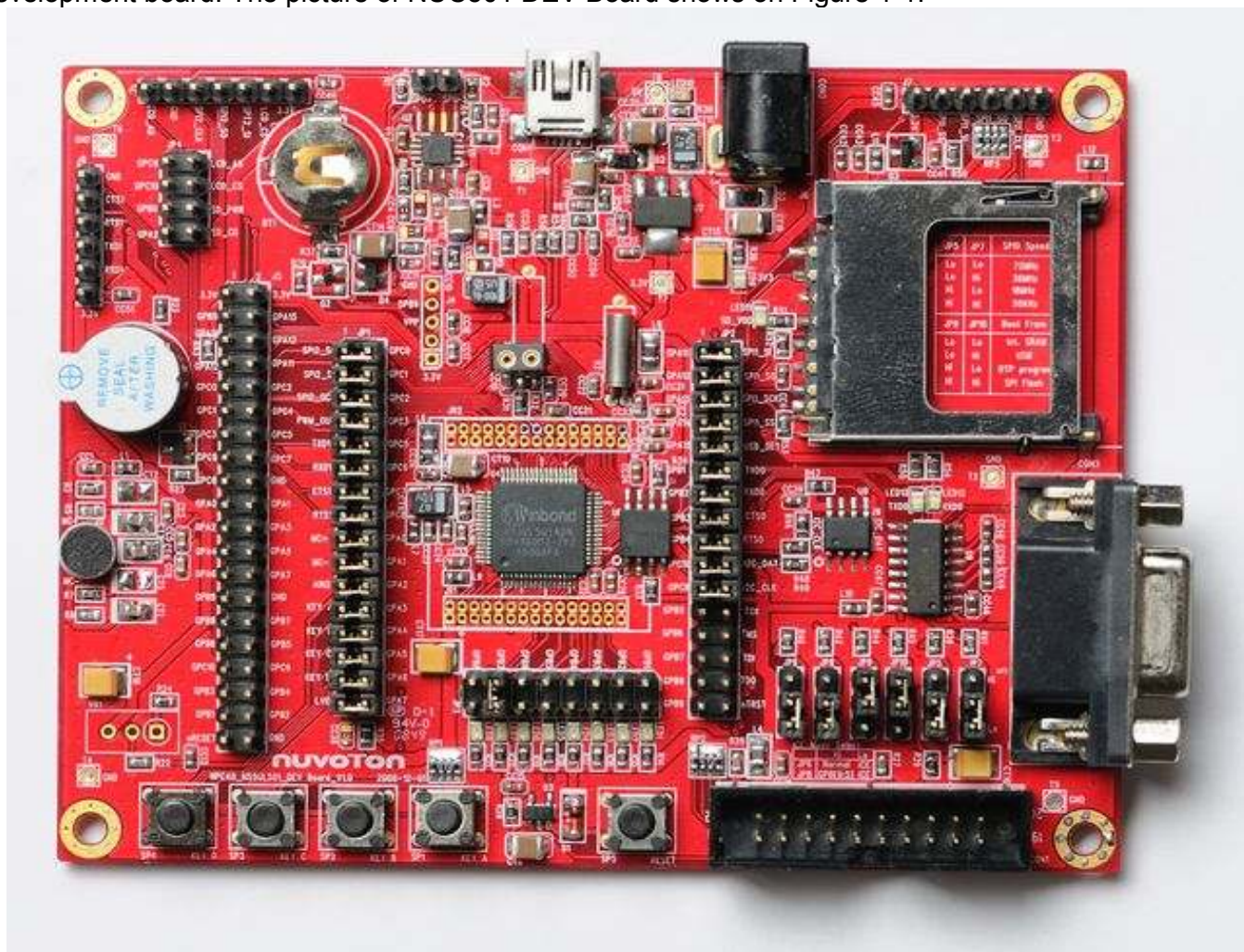


Figure 1-1 NUC501 Development board

32-BIT ARM7TDMI-BASED MCU

1.1 The NUC501 Development board

It was built around the Nuvoton's ARM7TDMI-based NUC501 MCU and provides versatile external devices such as one SPI flash for program and data storage, a SD card slot supported by SPI port1, one I²C interface serial EEPROM, two UART ports with one RS-232 level shifter for console connection (UART Port0) and one 20-pin JTAG interface for ICE debugging.

Each GPIO pin has dedicated jumper for function selection and all are connected to a 40-pin male connector which provides users an easy way to build up application system based on this development board.

Following listed the main components of NUC501 development board:

Main Components:

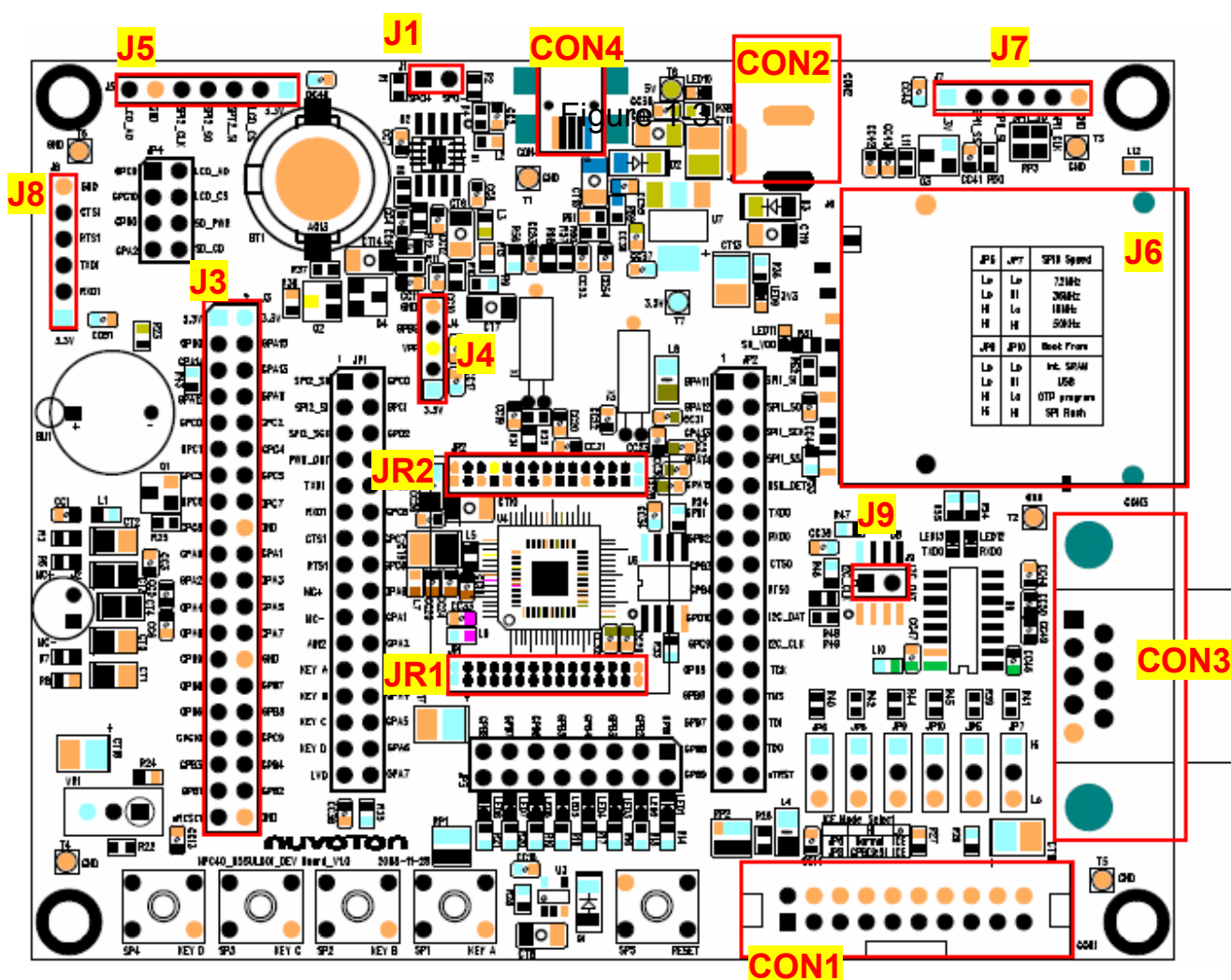
1. **MCU:** Nuvoton's ARM7TDMI-based NUC501, it can run up to 108MHz operating speed.
2. **GPIO extension slot:** One GPIO slot supports all the GPIO pins interface.
3. **AUDIO:** Onboard MIC input and mono AUDIO output with AMP.
4. **I²C EEPROM:** On board 24LC64 I²C E²PROMs.
5. **SPI FLASH:** On board 25X40 SPI serial FLASH for program storage.
6. **UART:** One UART port with Female type DSUB-9 connector.
7. **SD card Slot:** One SD card connector supported by SPI port1.
8. **JTAG connector:** One 20-pin JTAG ICE port for ICE connection.
9. **Key array:** 4-key array supported by GPA3~6.
10. **LED display:** Eight LED indicators connected to GPIO port B (High drive).
11. **DC power jack:** Please apply 5V/1A power adapter to CON6.
12. **LDO:** A 5V to 3.3V/1A LDO supports NUC501 and other 3.3v devices.

32-BIT ARM7TDMI-BASED MCU

1.1.1 DEV Board layout and connectors location

The following section provides board layout and peripheral connectors' information for using NUC501 DEV board. Below, shows the connectors' location of NUC501 DEV board on Figure 1-2.

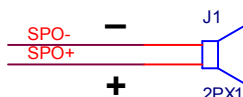
Figure 1-2 NUC501 Development board's layout



32-BIT ARM7TDMI-BASED MCU

AUDIO out connector: J1

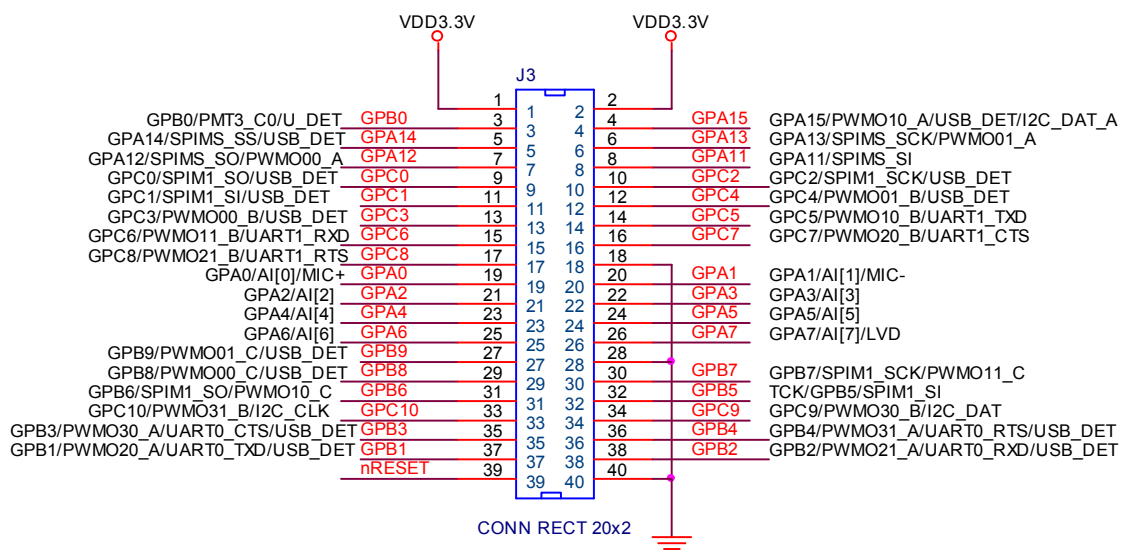
- Mono 16-bit Sigma-Delta DAC output



GPIO extension interface: J3

- 40 pin interface supports power, ground, reset and all GPIO pins interface.

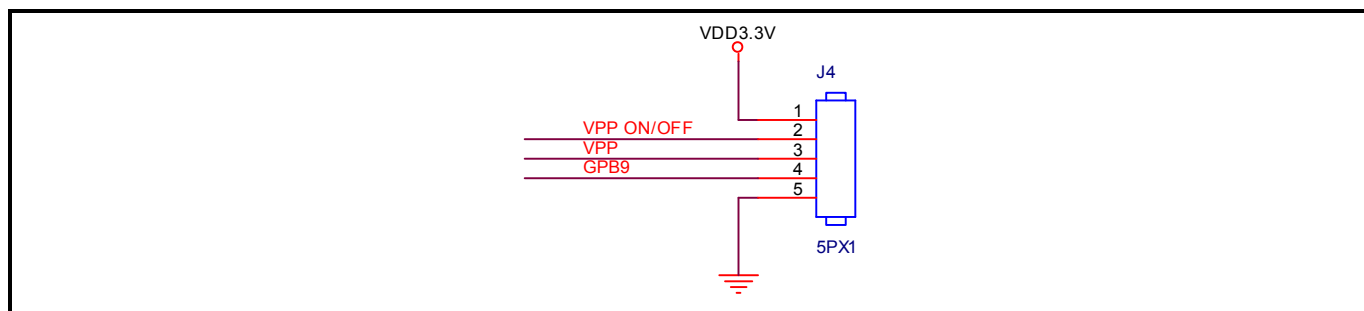
GPIO Extension Slot



32-BIT ARM7TDMI-BASED MCU

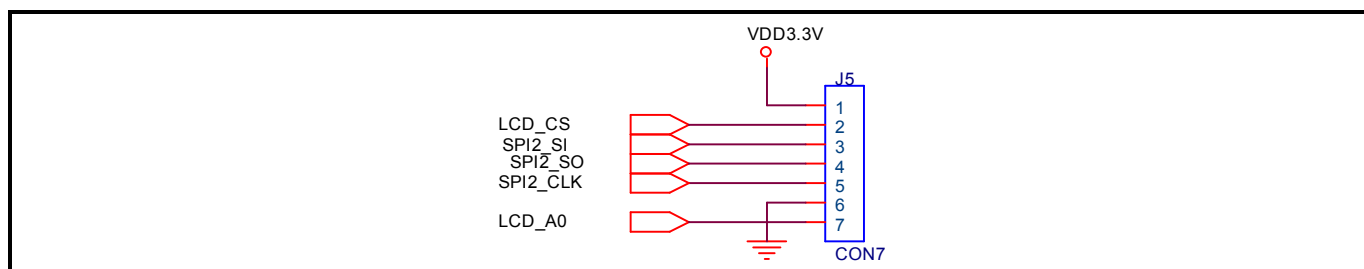
VPP supplier board interface: J4

- 5 pins interface for connecting VPP supplier board. It's for OTP memory burning use.



SPI Port 2 connector: J5

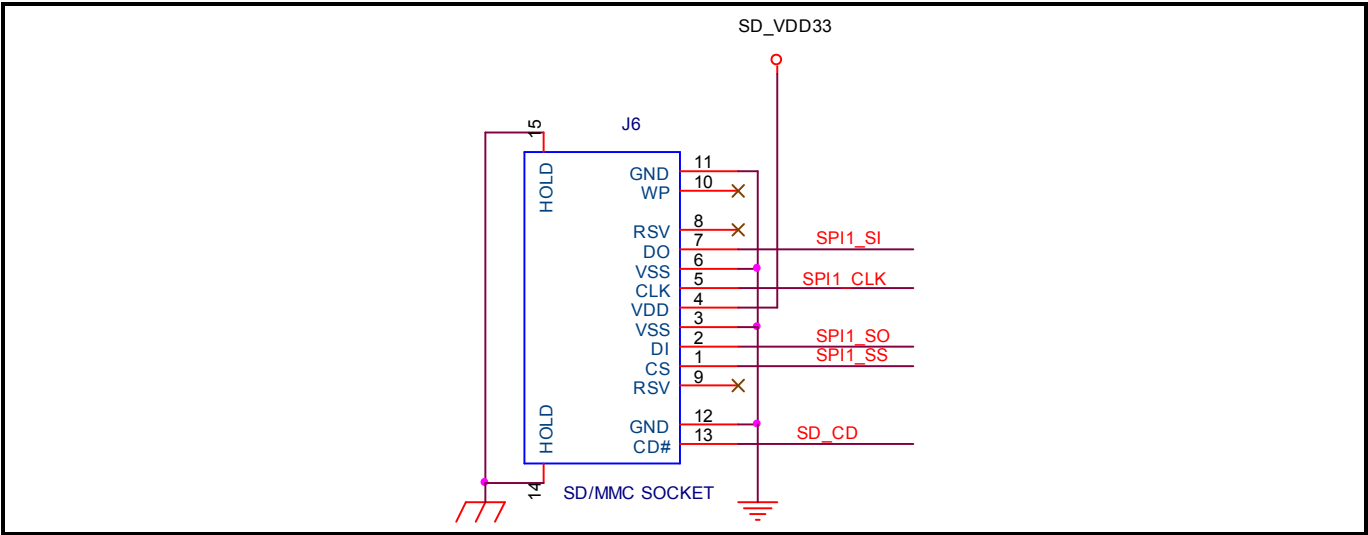
- SPI Port 2 interface + two I/O pins for MPU type LCM connection.



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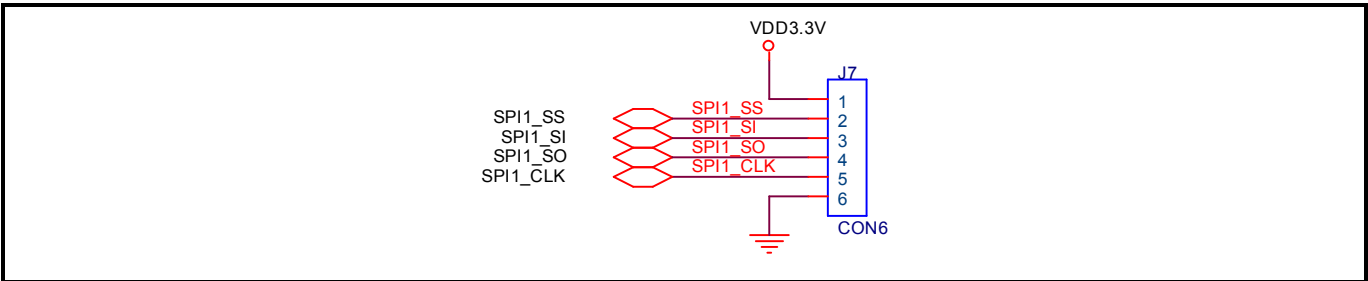
SD card slot: J6

- SD card interface (SPI mode only) connected to SPI port1.



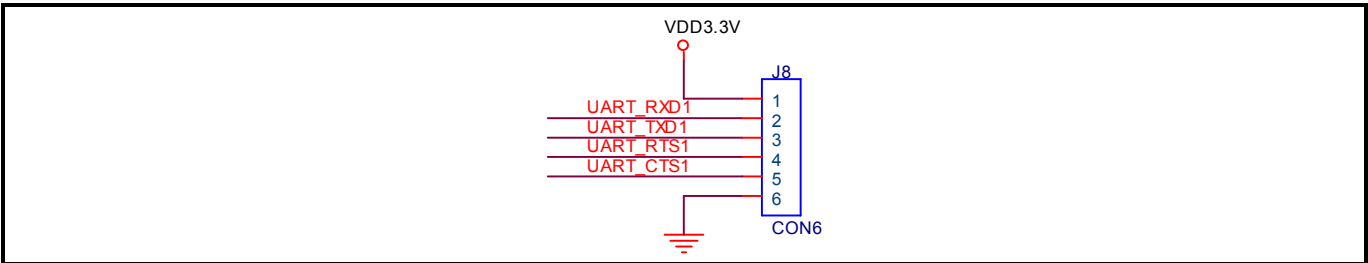
SPI Port 1 connector: J7

- SPI port 1 shared with SD card interface.



UART Port1 connector: J8

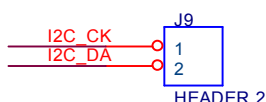
- UART port1 with CTS/RTS flow control interface. No level shifter supported onboard for RS-232 level shifting.



32-BIT ARM7TDMI-BASED MCU

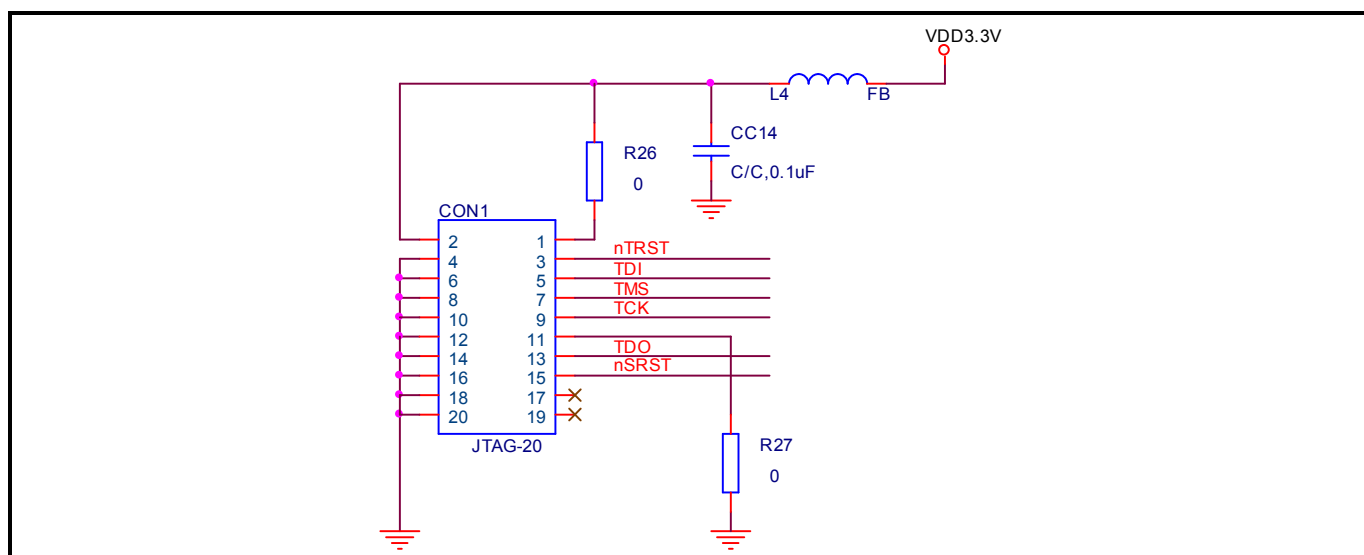
I2C connector: J9

- I2C signals, connected to an EEPROM 24LC64 onboard.



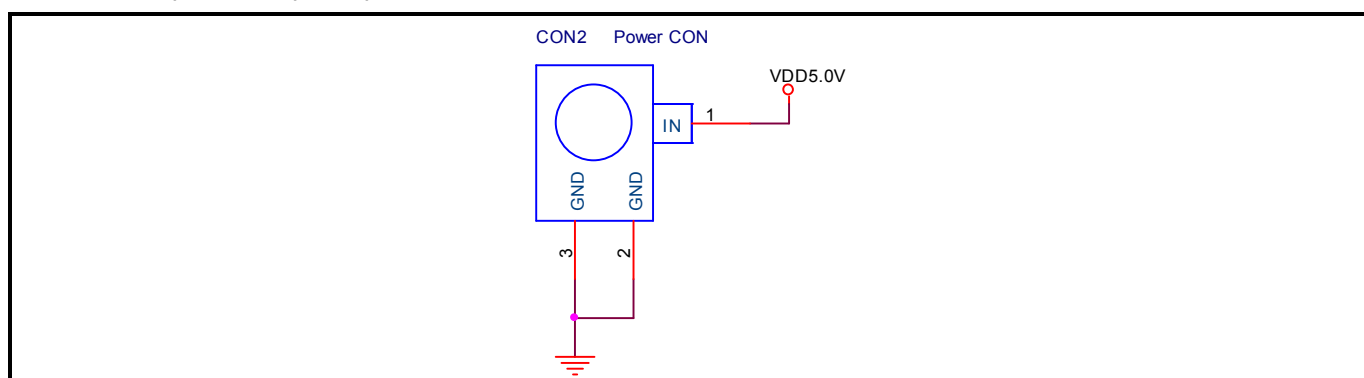
20-way JTAG connector: CON1

- 20-way JTAG interface.



Power adapter input: CON2

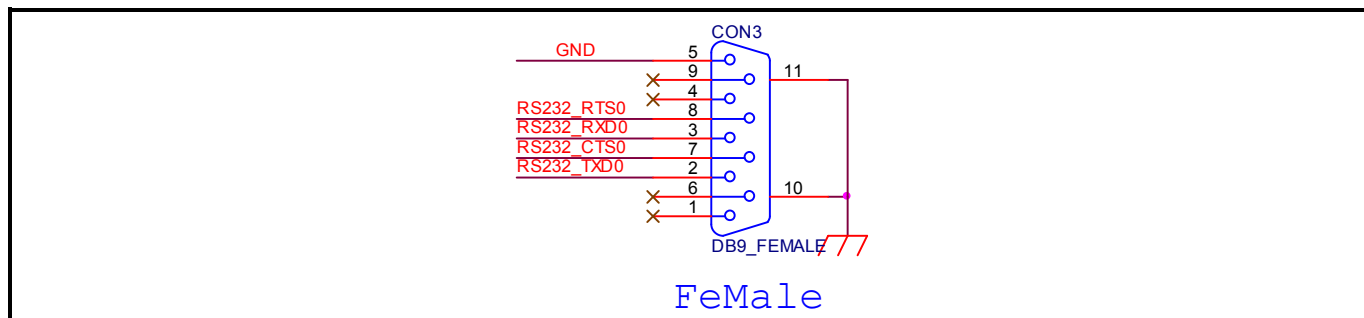
- 5V/1A power adapter input connector.



UART Port 0 connector: CON3

32-BIT ARM7TDMI-BASED MCU

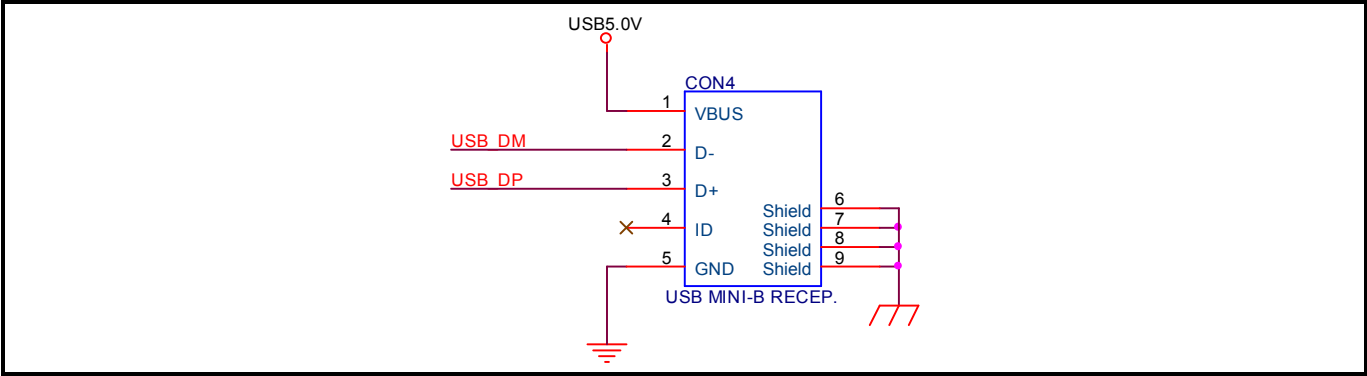
- UART port 0 with RS-232 level shifter for debug console.



32-BIT ARM7TDMI-BASED MCU

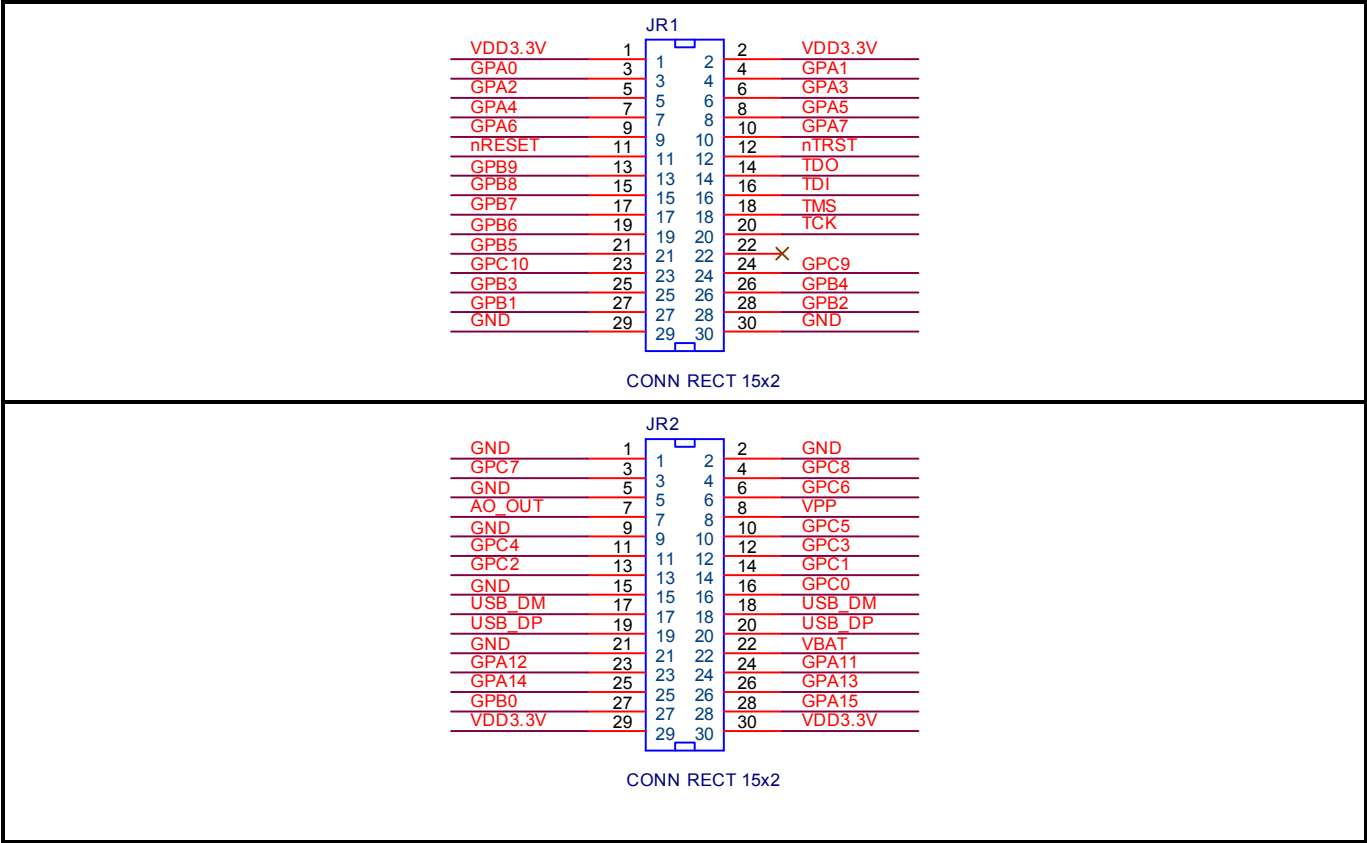
USB Device connector: CON4

- Mini-B type USB connector. USB BUS power can be the main power source for whole system.



NUC501AD Target module interface: JR1, JR2

- Total 60 pins interface for NUC501AD target module board connection.



32-BIT ARM7TDMI-BASED MCU

1.2 The NUC501AD Target Board

It provides NUC501AD LQFP48 package chip, 12MHz and 32.768 KHz crystals and SPI booting flash. All GPIO signals connected to 60-pin interface connector JR1 and JR2 to provide user an easy way to build-up development system. Please refer below picture for NUC501AD CPU board on Figure 1-3.



Figure 1-3

32-BIT ARM7TDMI-BASED MCU

1.2.1 Target Board layout and connectors

The following section provides NUC501AD Target board layout and peripheral connector information. Below, shows the connectors' location on Figure 1-4.

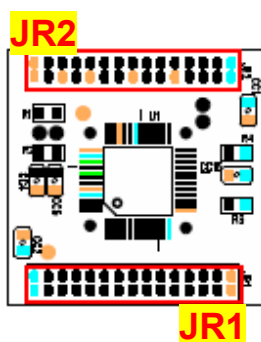


Figure 1-4

DEV board interface: JR1, JR2

- 60 pins interface for DEV board connection.

JR1					
VDD	1	1	2	VDD	2
GPA0	3	3	4	GPA1	4
GPA2	5	5	6	GPA3	6
GPA4	7	7	8	GPA5	8
GPA6	9	9	10	GPA7	10
nRESET	11	11	12		12
GPB9	13	13	14		14
GPB8	15	15	16		16
GPB7	17	17	18		18
GPB6	19	19	20		20
GPB5	21	19	20		22
	23	21	22		24
GPB3	25	23	24	GPB4	26
GPB1	27	25	26	GPB2	28
GND	29	27	28	GND	30
		29	30		
CONN RECT 15x2					

JR2					
GND	1	1	2	GND	2
	3	3	4		4
GND	5	5	6		6
AO_OUT	7	7	8	VPP	8
GND	9	9	10		10
	11	9	10		12
	13	11	12		14
	15	13	14		16
GND	17	15	16	USB_DM	18
USB_DM	19	17	18	USB_DP	20
USB_DP	21	19	20	VBAT	22
GND	23	21	22	GPA11	24
GPA12	25	23	24	GPA13	26
GPA14	27	25	26	GPA15	28
GPB0	29	27	28	VDD	30
VDD		29	30		
CONN RECT 15x2					

32-BIT ARM7TDMI-BASED MCU

1.3 The VPP Supplier Board

It provides the 6.5V and 1.8V voltage for OTP memory burning. GPB9 is the voltage control pin that high signal switching this board to supply 6.5V for OTP burning and low signal switching this board to supply 1.8V voltage. Below, shows board picture on Figure 1-5.

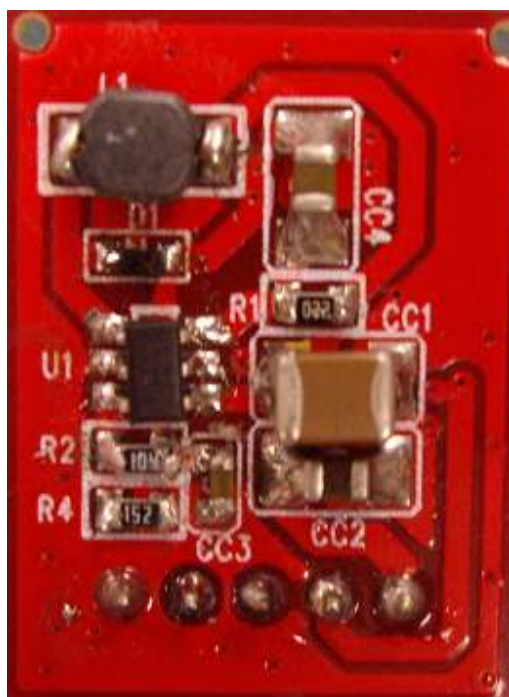


Figure 1-5 VPP supplier board

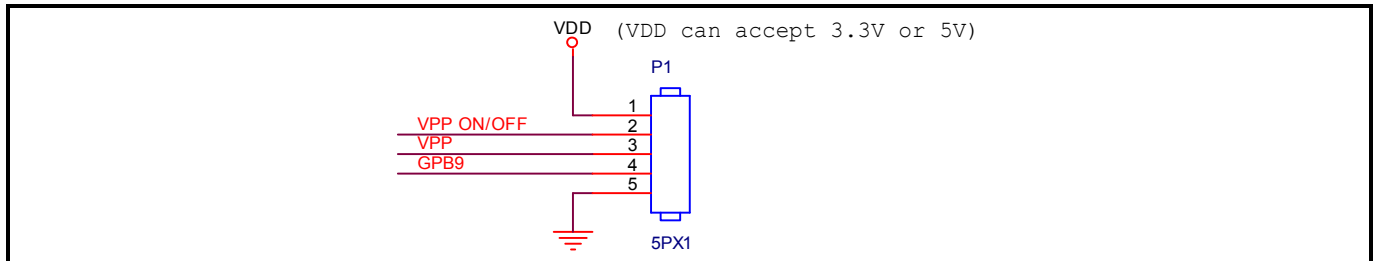
1.3.1 VPP Board layout and connectors

The following section provides VPP Supplier board layout and peripheral connector information. Below shows the connectors location on Figure 1-8.

VPP Supplier interface: P1

- 5 pins interface for DEV board connection. VPP and VPP ON/OFF signals are shorted.

32-BIT ARM7TDMI-BASED MCU



32-BIT ARM7TDMI-BASED MCU

2 Getting Started

There are a few hardware jumpers need to be set for selecting corresponding configuration you want. The following sections provide multi-function I/O information and all the jumper settings for configuring your NUC501 DEV board. Due to many IP function are sharing the same I/O pins in NUC501 series MCU, so please be carefully to set onboard jumpers to avoid conflict between functions.

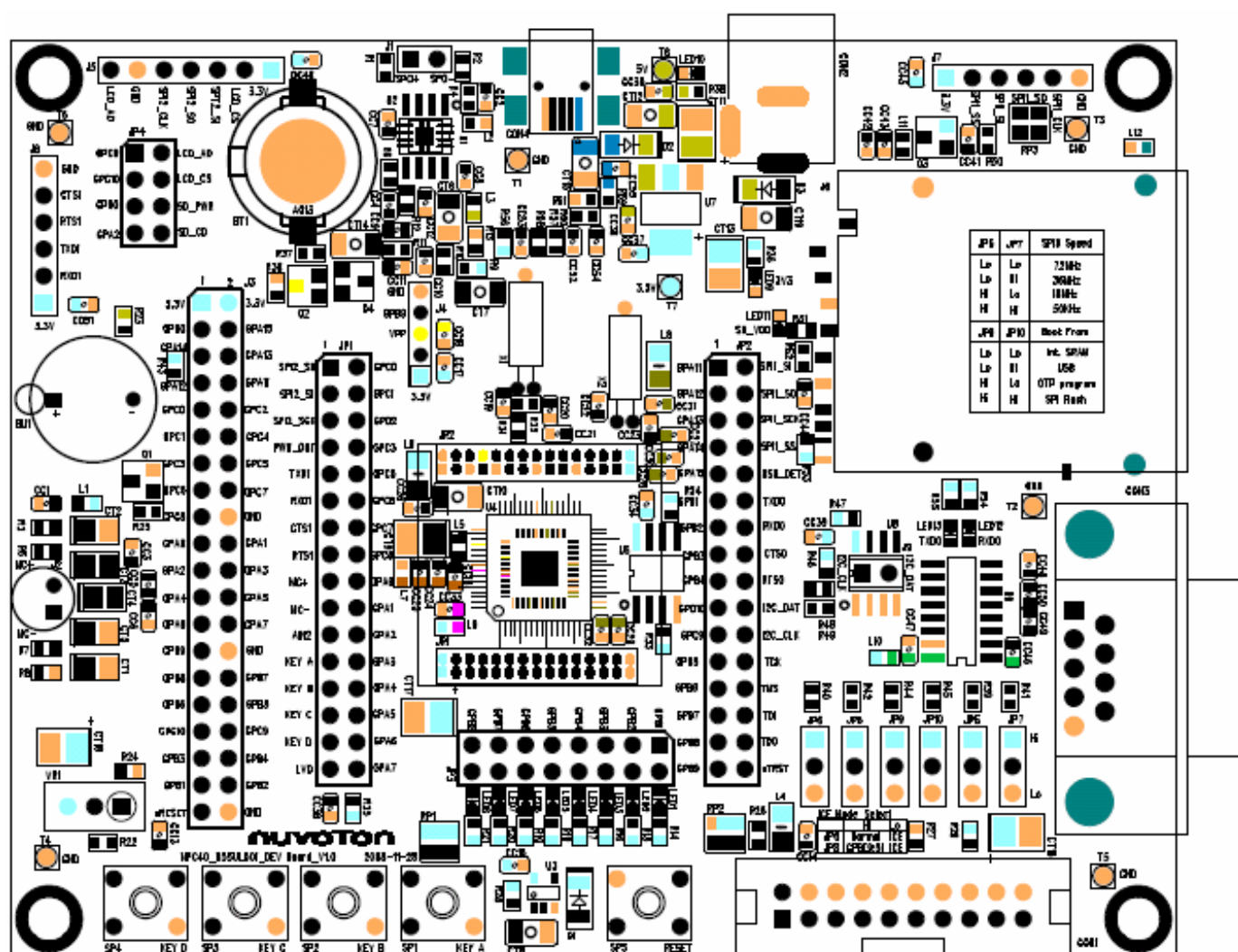


Figure 1-6 NUC501 Development board

32-BIT ARM7TDMI-BASED MCU

2.1 NUC501 I/O pin function list

GPA function list

Default Function Name	Alternative Function 1	Alternative Function 2	Alternative Function 3	Alternative Function 4
GPIO				
GPA[0]	AI[0]	MIC+		
GPA[1]	AI[1]	MIC-		
GPA[2]	AI[2]			
GPA[3]	AI[3]			
GPA[4]	AI[4]			
GPA[5]	AI[5]			
GPA[6]	AI[6]			
GPA[7]	AI[7]	LVD		
	SPI0_SS(Master)			
GPA[8]	SPI0_SCK			Power on set (IBR)
GPA[9]	SPI0_SO			Power on set (IBR)
GPA[10]	SPI0_SI			
GPA[11]	SPI1_SI			
GPA[12]	SPI1_SO	PWMO00_A		Power on set (IBR)
GPA[13]	SPI1_SCK	PWMO01_A		Power on set (48/64)
GPA[14]	SPI1_SS(Slave)	USB_DET		
GPA[15]	PWMO10_A	USB_DET	I2C_DATA_A	

32-BIT ARM7TDMI-BASED MCU

GPB function list

Default Function Name	Alternative Function 1	Alternative Function 2	Alternative Function 3	Alternative Function 4
GPIO				
GPB[0]	PWMO11_A	USB_DET	I2C_CLK_A	
GPB[1]	PWMO20_A	USB_DET	UART0_TXD	Power on set (ICE)
GPB[2]	PWMO21_A	USB_DET	UART0_RXD	
GPB[3]	PWMO30_A	USB_DET	UART0_CTS	
GPB[4]	PWMO31_A	USB_DET	UART0_RTS	Power on set (SPI_S0)
TCK	GPB[5]	SPI2_SI_A		
TMS	GPB[6]	SPI2_SO_A	PWMO10_C	
TDI	GPB[7]	SPI2_SCK_A	PWMO11_C	
TDO	GPB[8]	USB_DET	PWMO00_C	Power on set (SPI_S1)
nTRST	GPB[9]	USB_DET	PWMO01_C	

GPC function list

Default Function Name	Alternative Function 1	Alternative Function 2	Alternative Function 3	Alternative Function 4
GPIO				
GPC[0]	SPI2_SO_B	USB_DET		
GPC[1]	SPI2_SI_B	USB_DET		
GPC[2]	SPI2_SCK_B	USB_DET		
GPC[3]	PWMO00_B	USB_DET		
GPC[4]	PWMO01_B	USB_DET		
GPC[5]	PWMO10_B	UART1_TXD		
GPC[6]	PWMO11_B	UART1_RXD		
GPC[7]	PWMO20_B	UART1_CTS		
GPC[8]	PWMO21_B	UART1_RTS		
GPC[9]	PWMO30_B	I2C_DATA_B		
GPC[10]	PWMO31_B	I2C_CLK_B		

32-BIT ARM7TDMI-BASED MCU

2.2 Jumper settings

The following section describes all the jumpers on NUC501 DEV board, NUC501AD CPU board and VPP supplier board.

2.2.1 Power-On Settings

The power-on setting is used to configure the chip to enter the specified state when the chip is power-up or reset. Since each pin of power-on-setting pins has an internal pulled-up resistor. If the application needs to set the configuration to "0", the proper pull-down resistor must be added for the relative configuration pins.

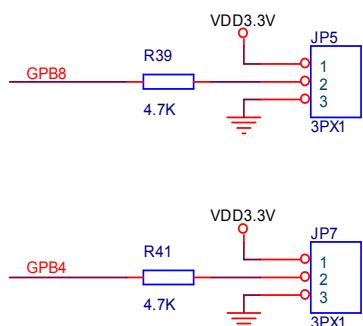
Pin Name	Descriptions	Register Bit Mapping
GPB[8] GPB[4]	SPI flash speed selection (SCLK) 00 : 72 MHz 01 : 36 MHz 10 : 18 MHz 11 : 50 KHz	SYS_CFG[6:5]
GPB[1]	<u>ICE Mode configuration setting</u> "0" ICE mode enable and the disable the cipher function "1" Normal mode	SYS_CFG[4]
GPA[13]	<u>LQFP48 ICE mode configuration setting</u> "0" 48-pins package and GPB[9:5] for ICE connection "1" 48-pins package and GPB[9:5] use the normal function	SYS_CFG[3]

32-BIT ARM7TDMI-BASED MCU

GPA[12] GPA[9] GPA[8]	<ul style="list-style-type: none"> • 3'b000 : SRAM BIST mode • 3'b001 : USB PHY test mode • 3'b010 : Analog test mode • 3'b011 : ARM7TDMI test mode • 3'b100 : Boot from SRAM • 3'b101 : Boot from USB • 3'b110 : OTP program mode • 3'b111 : Boot from SpiMemory 	SYS_CFG[2:0]
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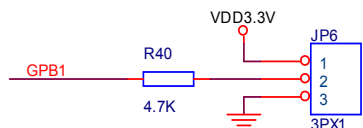
Following list the Power-on setting jumpers on NUC501 DEV board. Please mapping to above table for power-on mode configuration.

SPI0 Speed Configuration



GPB8/GPB4	SPI Speed
(0,0)	72MHz
(0,1)	36MHz
(1,0)	18MHz
(1,1)	50KHz

ICE Mode configuration setting

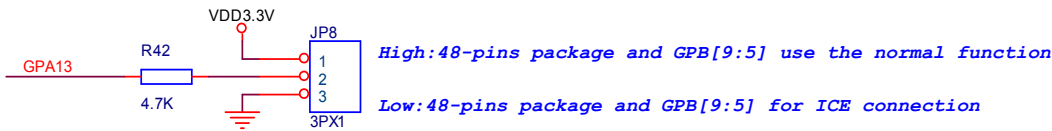


High:normal mode

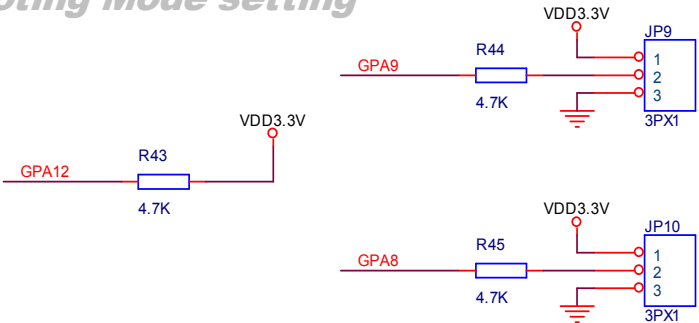
Low:ICE mode enable and the disable the cipher function

32-BIT ARM7TDMI-BASED MCU

LQFP48 ICE mode configuration setting



Booting Mode setting



GPA12=1 GPA9/GPA8	Function
(0/0)	Boot from SRAM
(0/1)	Boot from USB
(1/0)	OTP program mode
(1/1)	Boot from SPI

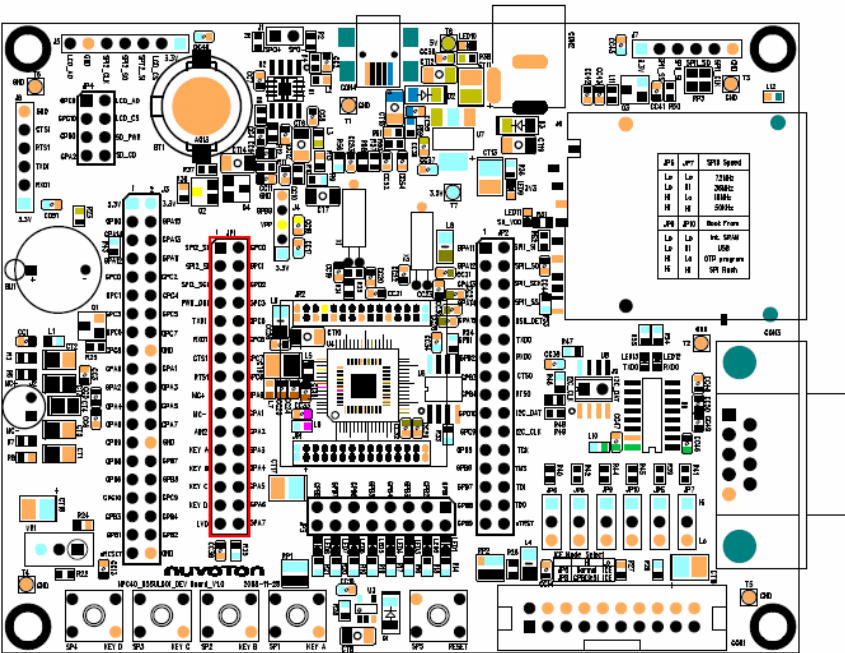


32-BIT ARM7TDMI-BASED MCU

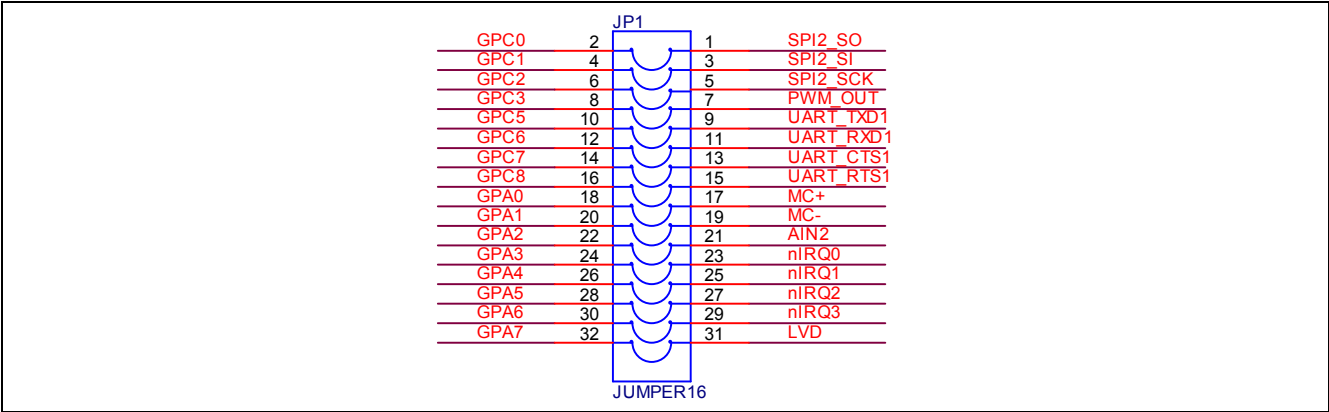
2.2.2 GPIO Jumpers

JP1 jumpers:

The jumpers group JP1 is for SPI port2, UART port1, nIRQ ,PWM_out and MIC input function, bellow describes the pin functions and location. Please make sure jumpers status when using those functions.



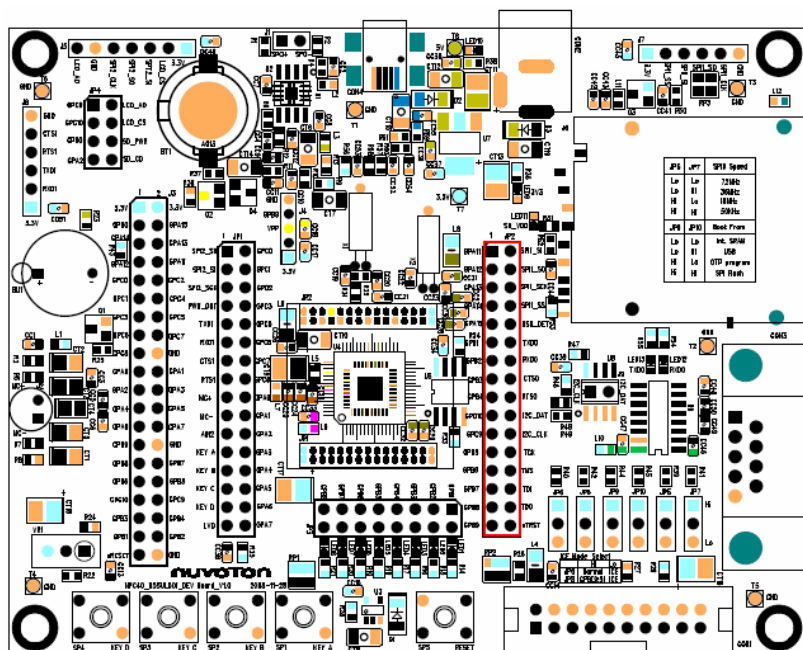
Jumper Open	Short 1-2
GPC0	SPI2_SO
GPC1	SPI2_SI
GPC2	SPI2_SCK
GPC3	PWM_OUT
GPC5	UART_TXD1
GPC6	UART_RXD1
GPC7	UART_CTS1
GPC8	UART_RTS1
GPA0	MC+
GPA1	MC-
GPA2	AIN2
GPA3	nIRQ0
GPA4	nIRQ1
GPA5	nIRQ2
GPA6	nIRQ3
GPA7	LVD



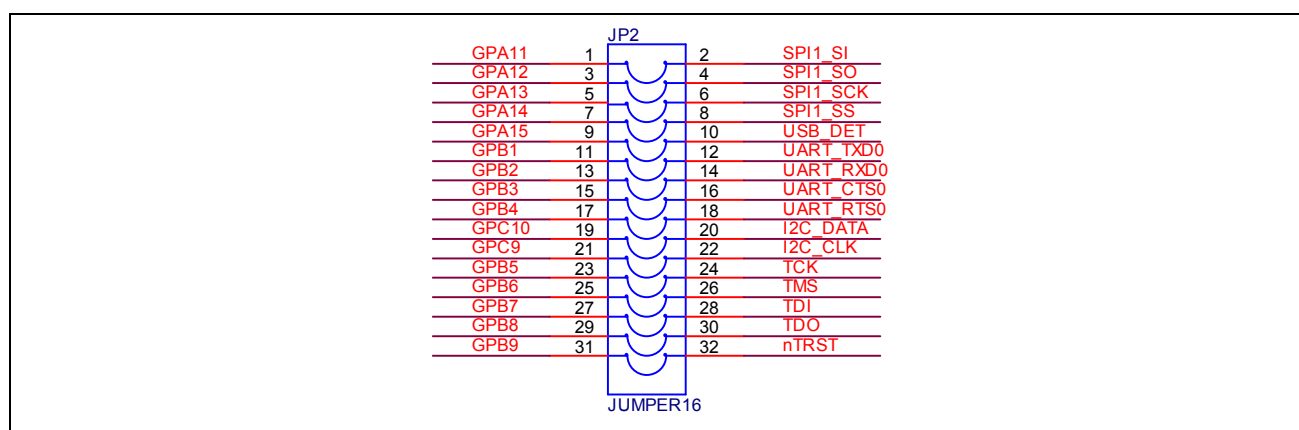
32-BIT ARM7TDMI-BASED MCU

JP2 jumpers:

The jumper group JP2 is for JTAG, SPI port1, UART port0, I2C and USB detection functions, bellow describes the pin functions and location. Please make sure jumpers status when using those functions.



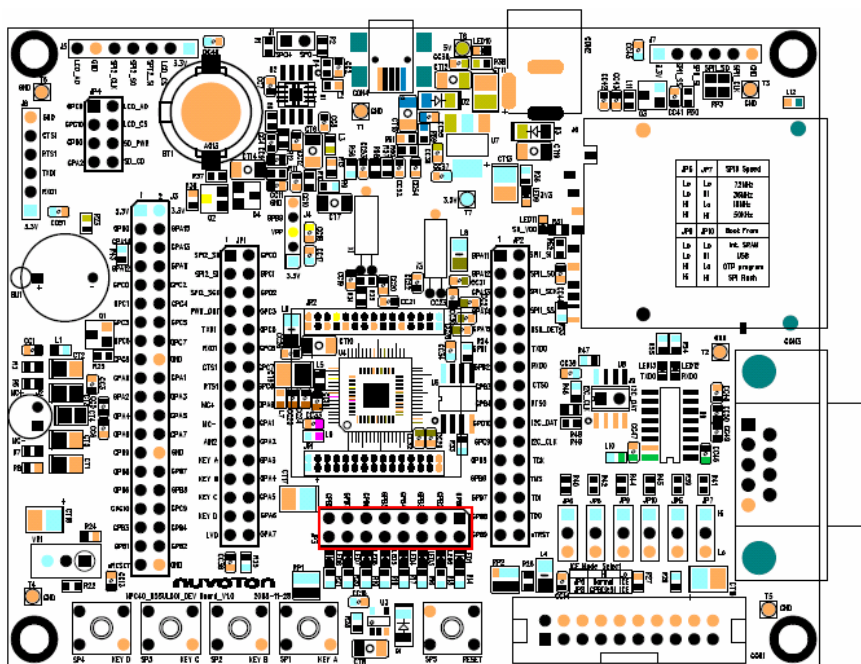
Jumper Open	Short 1-2
GPA11	SPI1_SI
GPA12	SPI1_SO
GPA13	SPI1_SCK
GPA14	SPI1_SS
GPA15	USB_DET
GPB1	UART_TXD0
GPB2	UART_RXD0
GPB3	UART_CTS0
GPB4	UART_RTS0
GPC10	I2C_DATA
GPC9	I2C_CLK
GPB5	TCK
GPB6	TMS
GPB7	TDI
GPB8	TDO
GPB9	nTRST



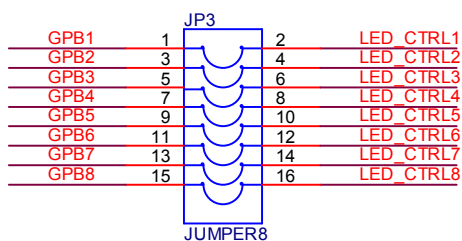
32-BIT ARM7TDMI-BASED MCU

JP3 jumpers:

The jumpers group JP3 is for LED indicators control settings, bellow describes the pin functions and location. Please make sure jumpers status when using those functions.



Jumper Open	Short 1-2
GPB1	LED_CTRL1
GPB2	LED_CTRL2
GPB3	LED_CTRL3
GPB4	LED_CTRL4
GPB5	LED_CTRL5
GPB6	LED_CTRL6
GPB7	LED_CTRL7
GPB8	LED_CTRL8

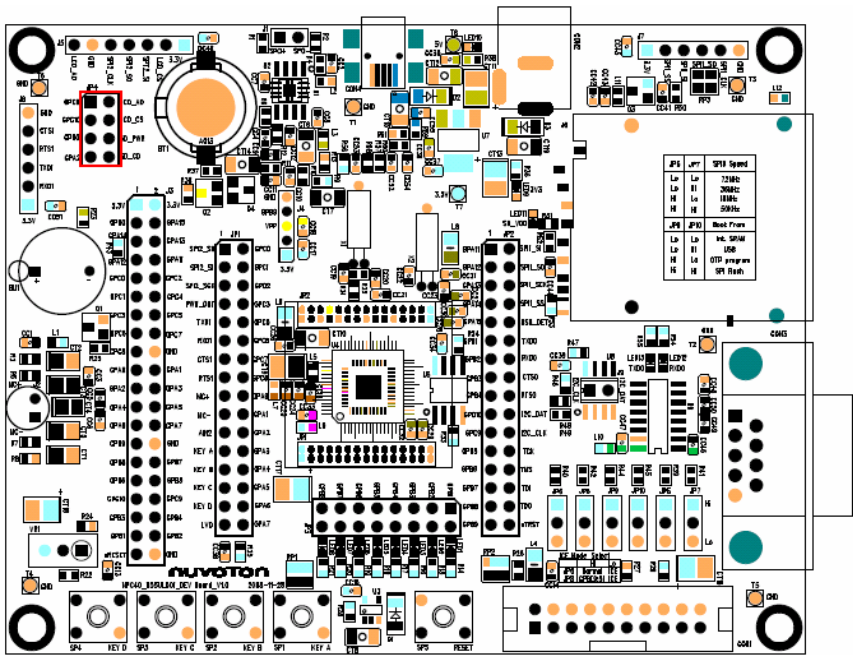




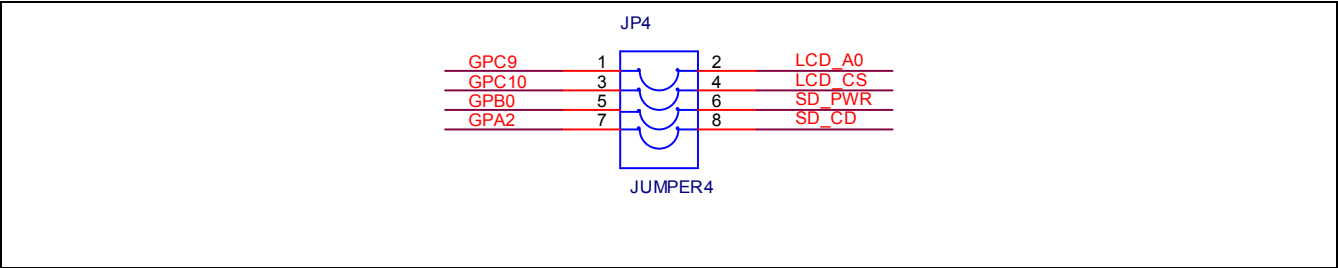
32-BIT ARM7TDMI-BASED MCU

JP4 jumpers:

The jumpers group JP4 is for LCD and SD card control signals settings, bellow describes the pin functions and location.



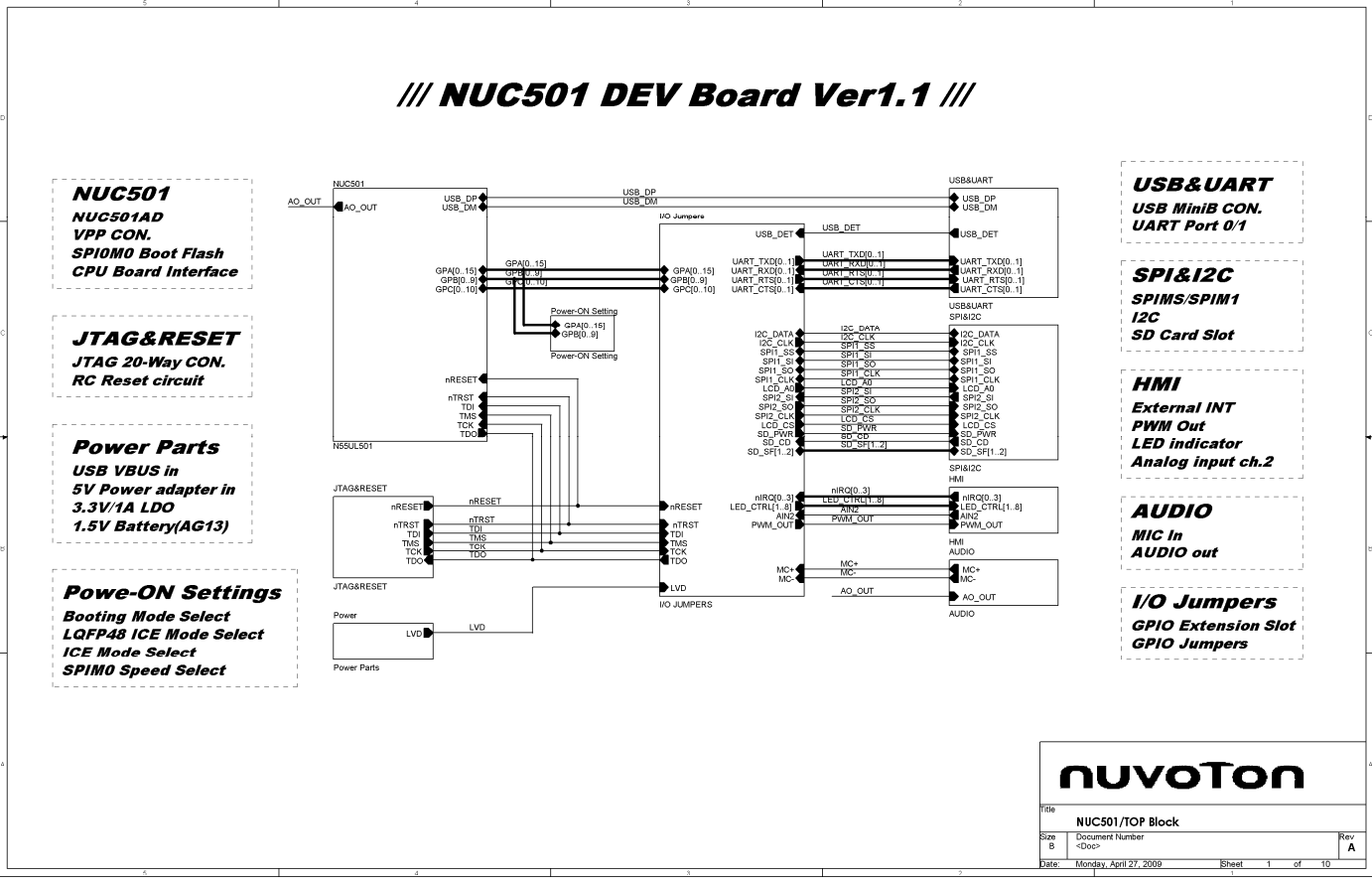
Jumper Open	Short 1-2
GPC9	LCD_A0
GPC10	LCD_CS
GPB0	SD_PWR
GPA2	SD_CD





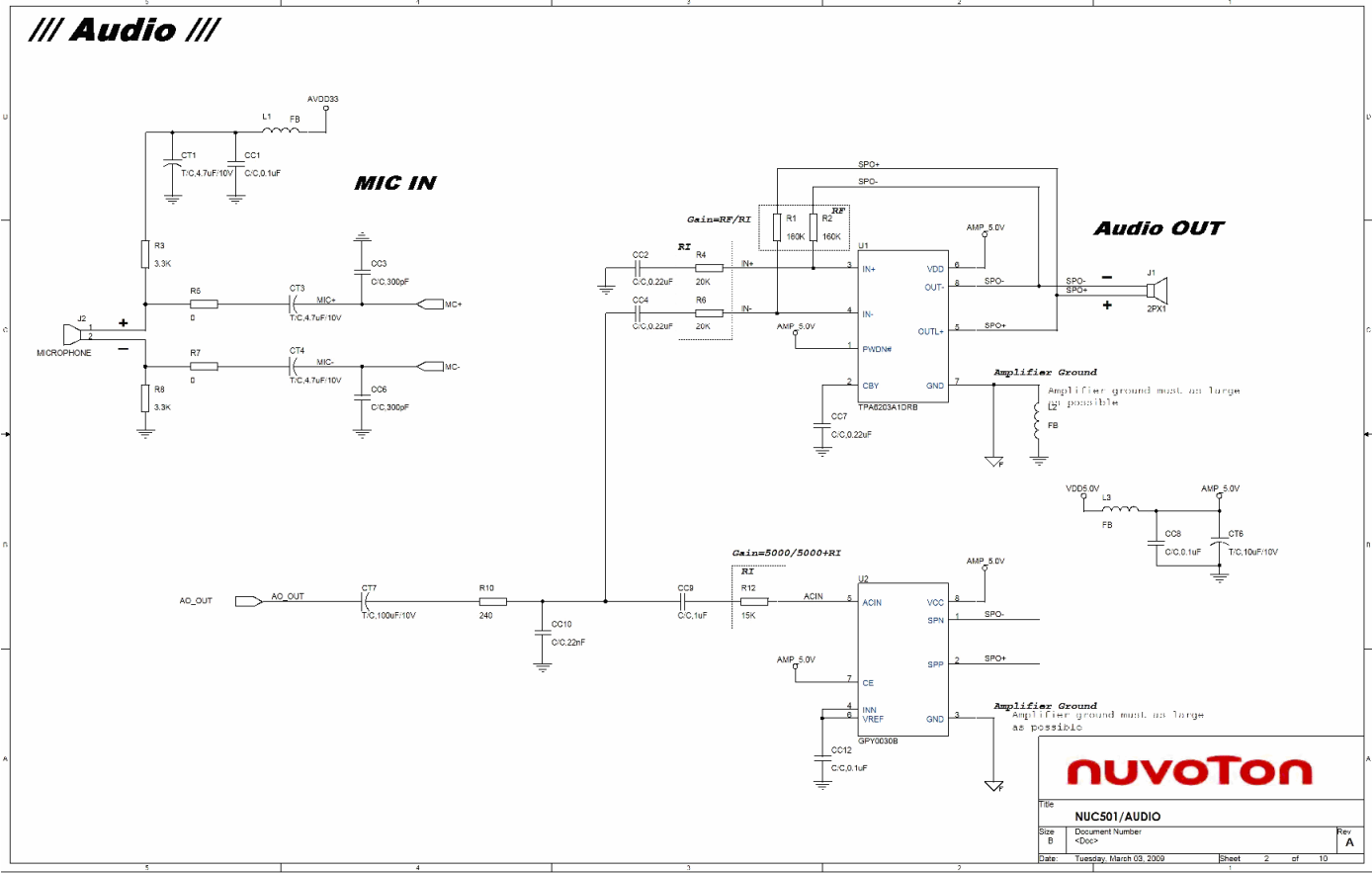
32-BIT ARM7TDMI-BASED MCU

3 Schematic



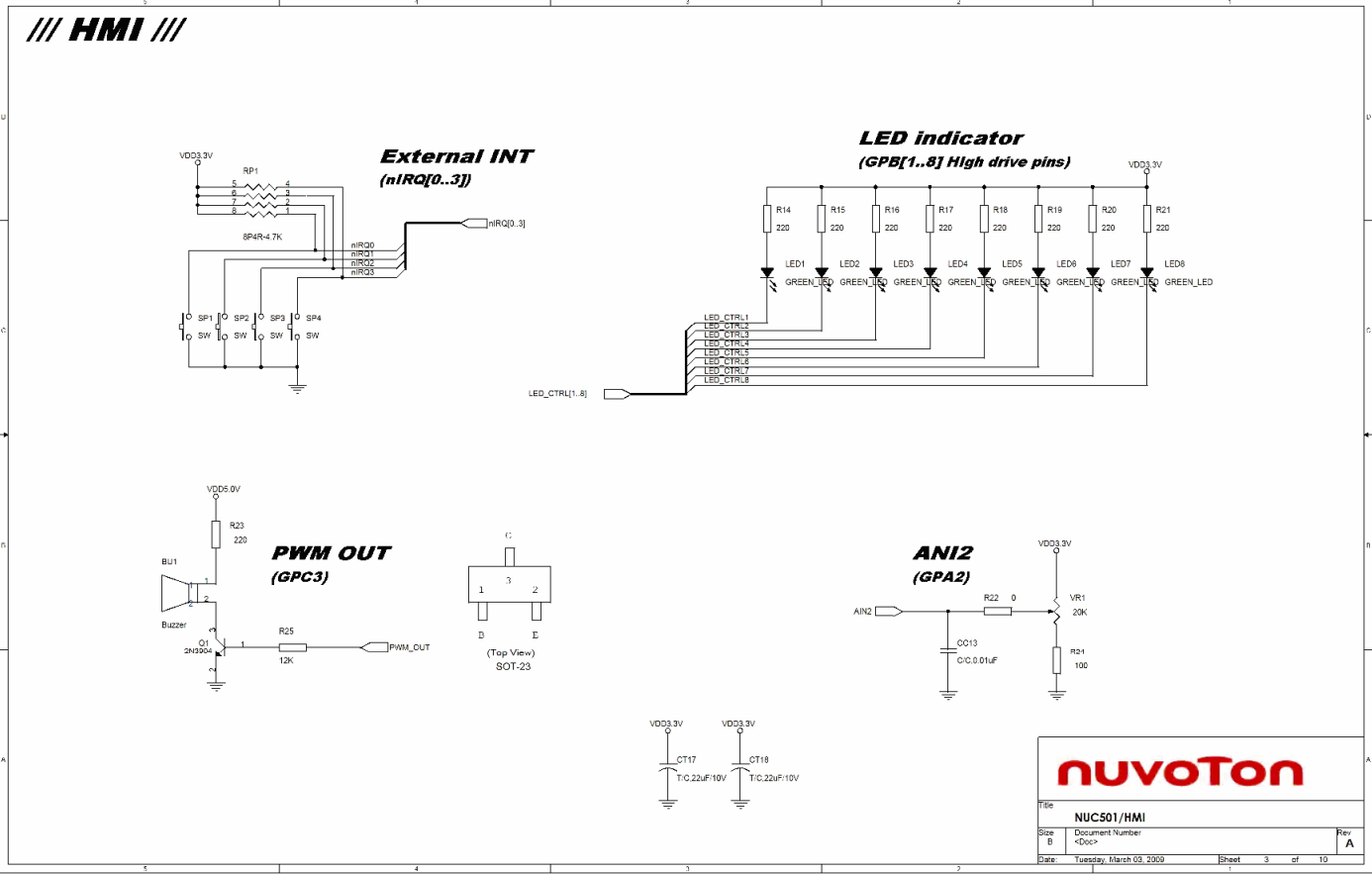


32-BIT ARM7TDMI-BASED MCU



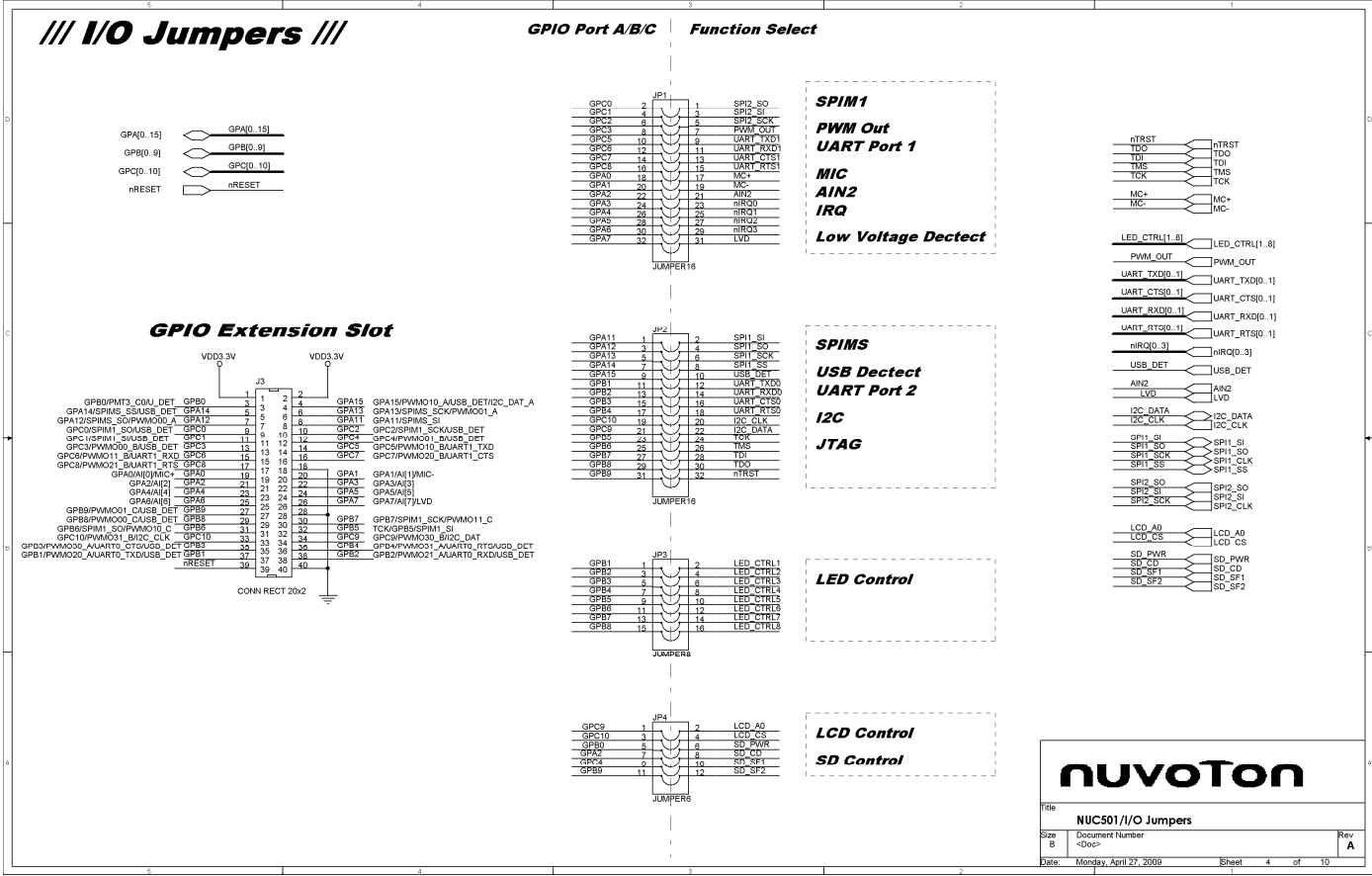


32-BIT ARM7TDMI-BASED MCU

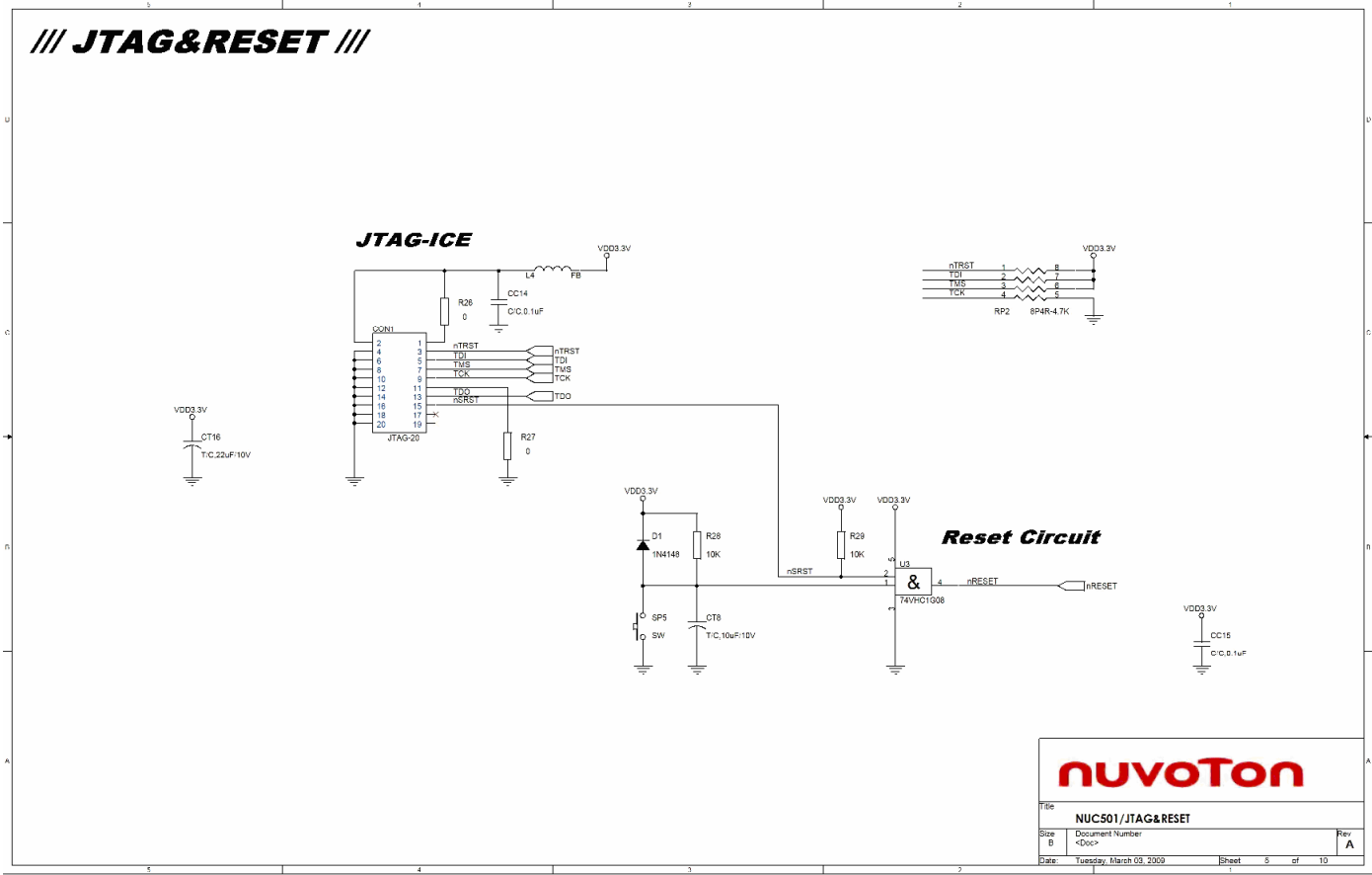




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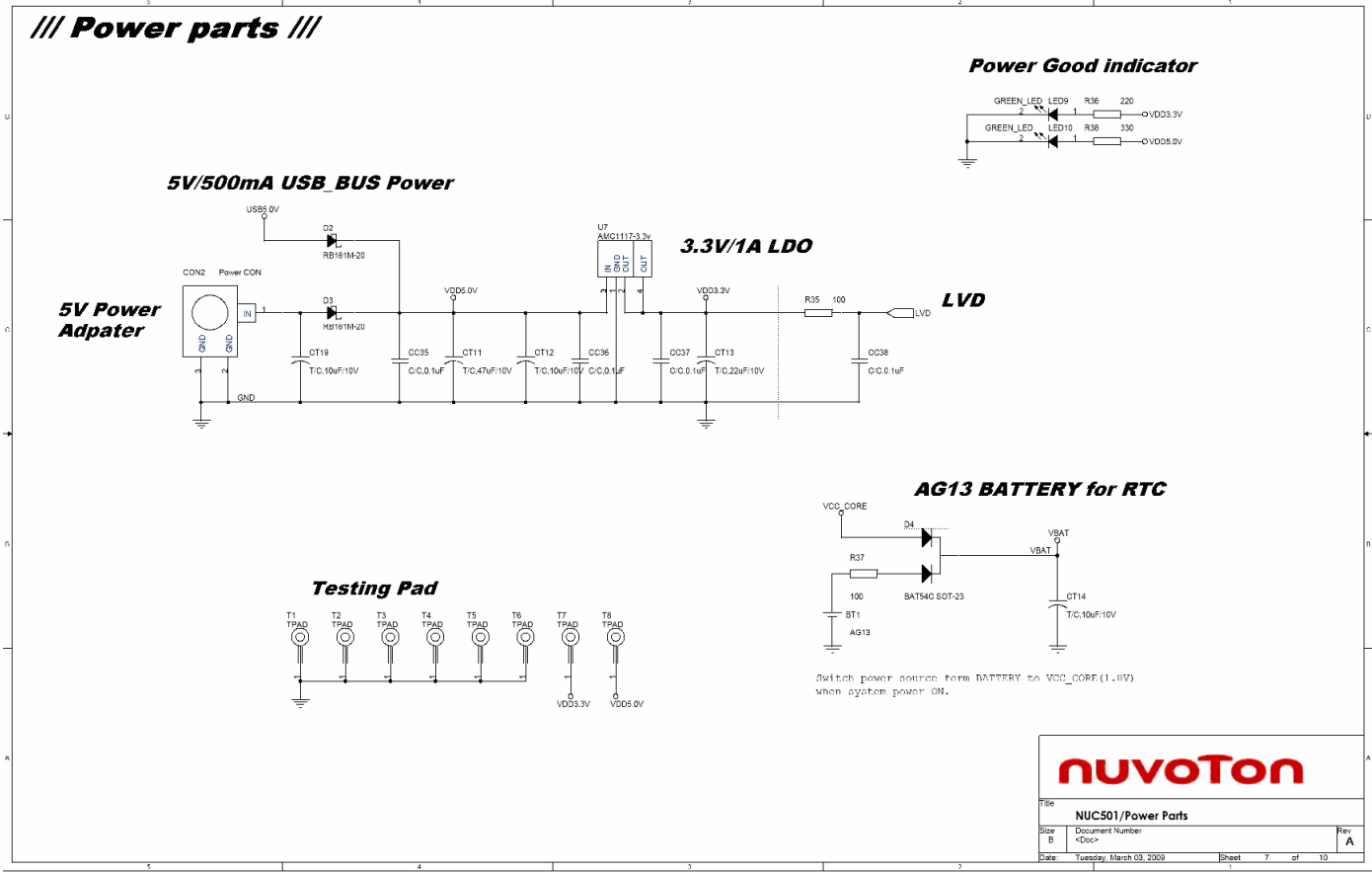


/// NUC501 ///



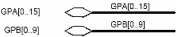


32-BIT ARM7TDMI-BASED MCU

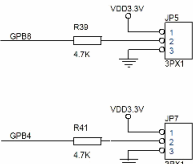


32-BIT ARM7TDMI-BASED MCU

/// Power-ON Settings ///

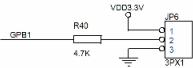


SPI0 Speed Configuration



GPB6/GPB4	SPI Speed
(0,0)	72MHz
(0,1)	36MHz
(1,0)	18MHz
(1,1)	9MHz

ICE Mode configuration setting



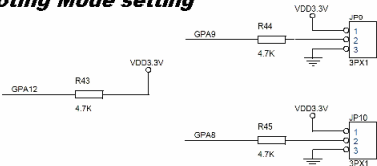
High: normal mode
Low: ICE mode enable and the disable the cipher function

LQFP48 ICE mode configuration setting



High: 48-pins package and GPB[9:5] use the normal function
Low: 48-pins package and GPB[9:5] for ICE connection

Booting Mode setting



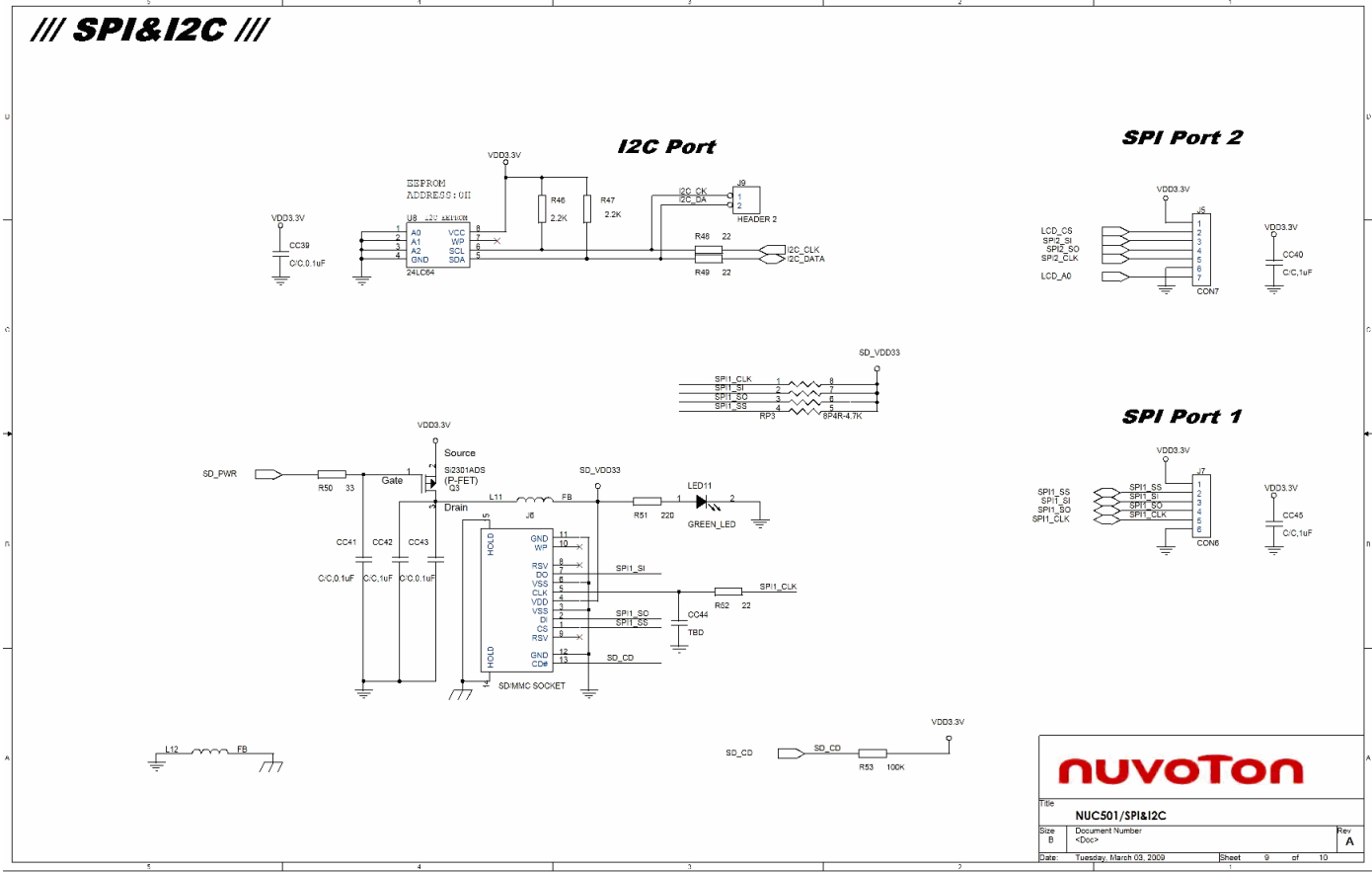
SELECT GPA9/GPA8	Function
(0/0)	Boot from SRAM
(0/1)	Boot from USB
(1/0)	OTP program mode
(1/1)	Boot from SPI

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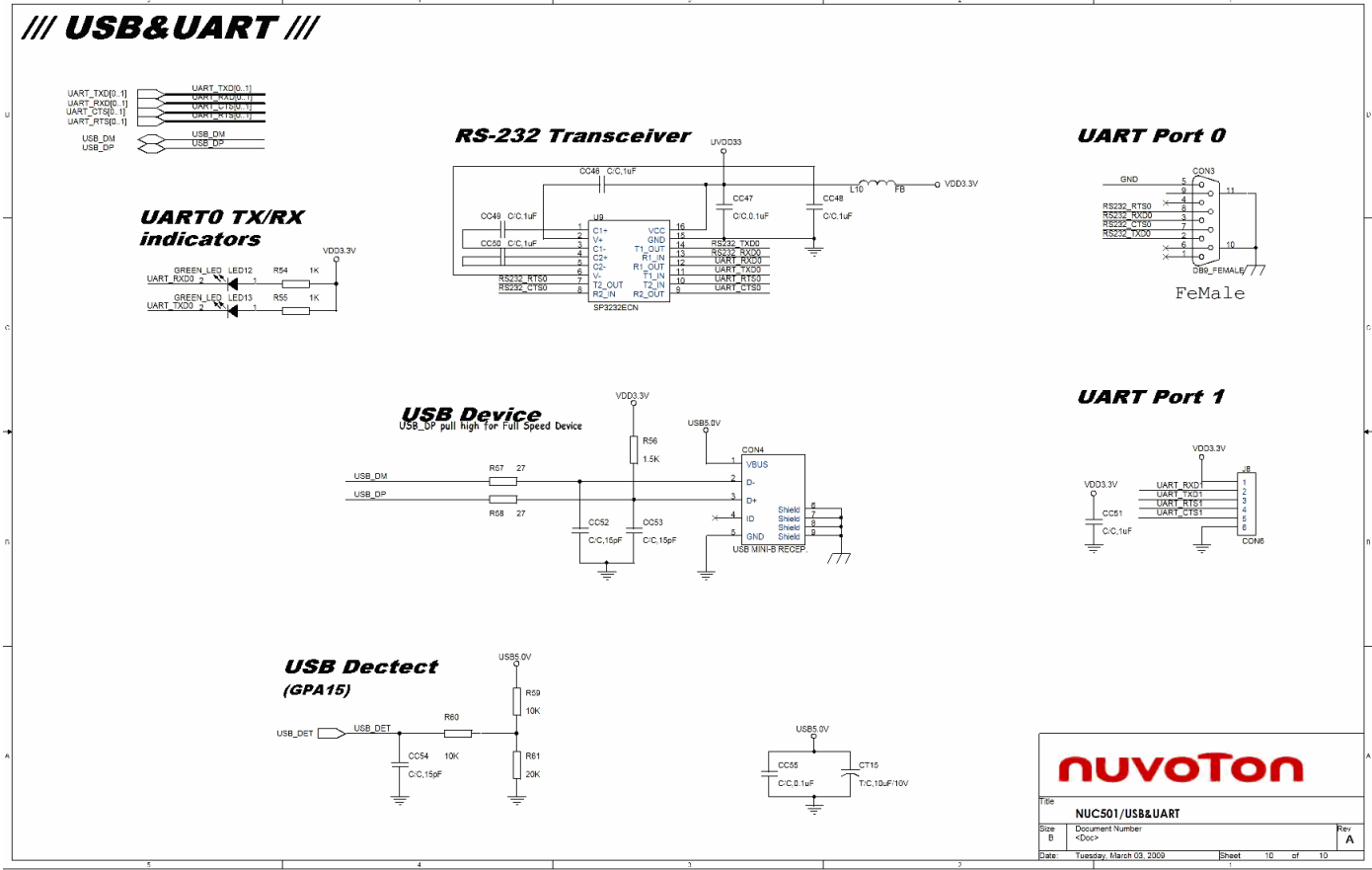
File		
NUC501/Power-ON Settings		
Size	Document Number	Rev
B	<Doc>	A
Date:	Tuesday, March 03, 2009	Sheet 8 of 10



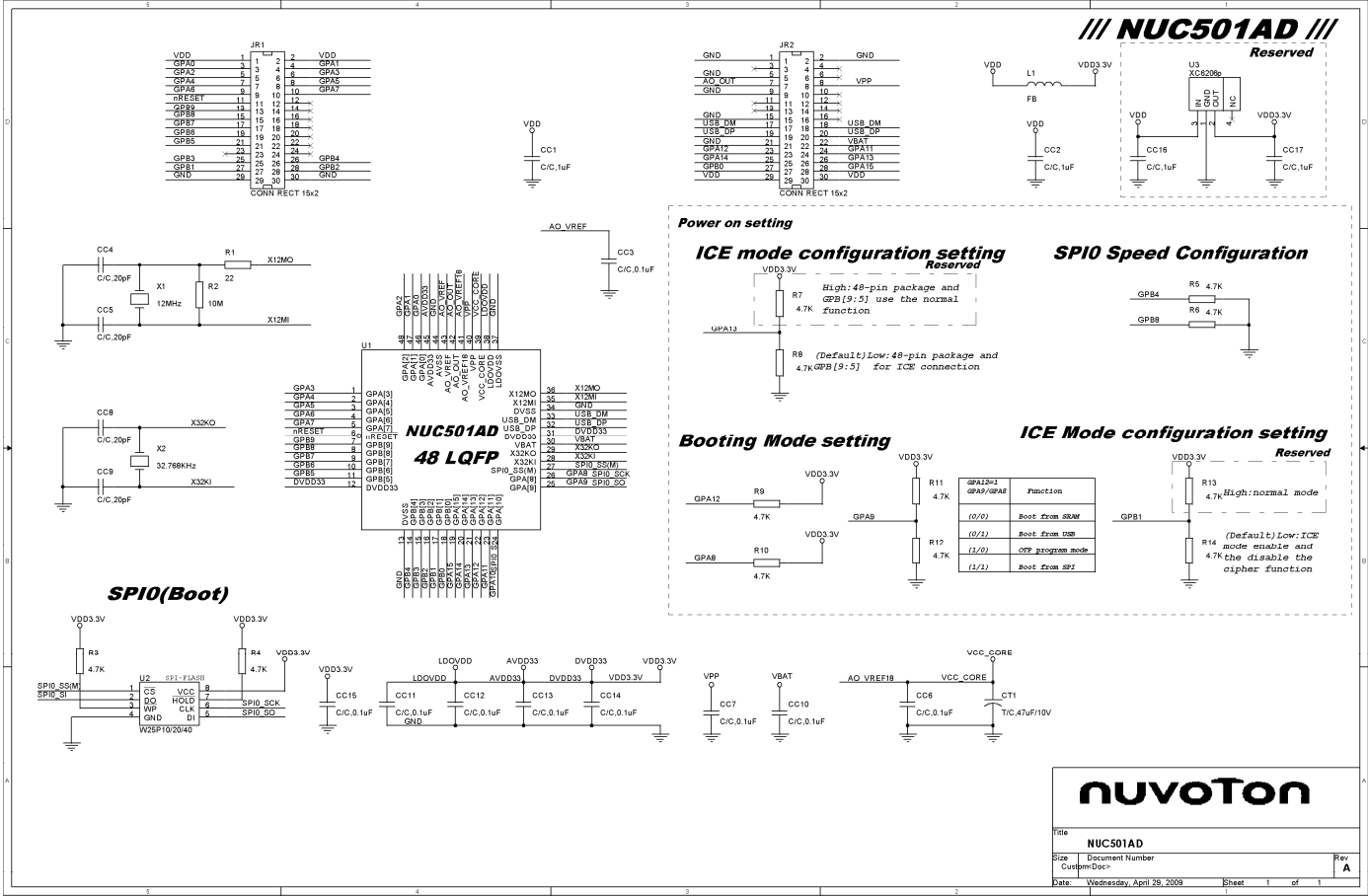
32-BIT ARM7TDMI-BASED MCU



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[illegible]



32-BIT ARM7TDMI-BASED MCU

4 BOM List

NUC501 Development Board BOM List:

NUC501/TOP Block Revised: Friday, March 06, 2009 Revision: A

Bill Of Materials March 13,2009 10:59:47 Page1

Item	Quantity	Reference	Part
1	1	BT1	AG13
2	1	BU1	Buzzer
3	25	CC1,CC8,CC12,CC14,CC15, CC16,CC21,CC24,CC26,CC27, CC28,CC29,CC30,CC31,CC33, CC34,CC35,CC36,CC37,CC38, CC39,CC41,CC43,CC47,CC55	C/C,0.1uF
4	3	CC2,CC4,CC7	C/C,0.22uF
5	2	CC6,CC3	C/C,300pF
6	13	CC9,CC17,CC18,CC25,CC32, CC40,CC42,CC45,CC46,CC48, CC49,CC50,CC51	C/C,1uF
7	1	CC10	C/C,22nF
8	1	CC13	C/C,0.01uF
9	4	CC19,CC20,CC22,CC23	C/C,20pF
10	1	CC44	TBD
11	3	CC52,CC53,CC54	C/C,15pF
12	1	CON1	JTAG-20
13	1	CON2	Power CON
14	1	CON3	DB9_FEMALE
15	1	CON4	USB MINI-B RECEP.
16	3	CT1,CT3,CT4	T/C,4.7uF/10V
17	7	CT6,CT8,CT10,CT12,CT14, CT15,CT19	T/C,10uF/10V
18	1	CT7	T/C,100uF/10V
19	2	CT9,CT11	T/C,47uF/10V
20	4	CT13,CT16,CT17,CT18	T/C,22uF/10V
21	1	D1	1N4148
22	2	D2,D3	RB060L-40
23	1	D4	BAT54C SOT-23
24	2	JP1,JP2	JUMPER16
25	1	JP3	JUMPER8
26	1	JP4	JUMPER6
27	6	JP5,JP6,JP7,JP8,JP9,JP10	3PX1
28	2	JR1,JR2	CONN RECT 15x2
29	1	J1	2PX1

32-BIT ARM7TDMI-BASED MCU

30	1	J2	MICROPHONE	
31	1	J3	CONN RECT 20x2	
32	1	J4	5PX1	
33	1	J5	CON7	
34	1	J6	SD/MMC SOCKET	
35	2	J8,J7	CON6	
36	1	J9	HEADER 2	
37	13	LED1,LED2,LED3,LED4,LED5, LED6,LED7,LED8,LED9, LED10,LED11,LED12,LED13	GREEN_LED	
38	12	L1,L2,L3,L4,L5,L6,L7,L8, FB L9,L10,L11,L12		
39	1	Q1	2N3904	
40	2	Q3,Q2	Si2301ADS	
41	3	RP1,RP2,RP3	8P4R-4.7K	
42	2	R2,R1	160K	
43	2	R8,R3	3.3K	
44	4	VR1,R4,R6,R61	20K	
45	5	R5,R7,R22,R26,R27	0	
46	1	R10	240	
47	1	R12	15K	
48	11	R14,R15,R16,R17,R18,R19, R20,R21,R23,R36,R51	220	
49	3	R24,R35,R37	100	
50	1	R25	12K	
51	5	R28,R29,R30,R59,R60	10K	
52	4	R31,R48,R49,R52	22	
53	1	R32	10M	
54	9	R33,R34,R39,R40,R41,R42, R43,R44,R45	4.7K	
55	1	R38	330	
56	2	R47,R46	2.2K	
57	1	R50	33	
58	1	R53	100K	
59	2	R55,R54	1K	
60	1	R56	1.5K	
61	2	R57,R58	27	
62	5	SP1,SP2,SP3,SP4,SP5	SW	
63	8	T1,T2,T3,T4,T5,T6,T7,T8	TPAD	
64	1	U1	TPA6203A1DRB	
65	1	U2	GPY0030B	
66	1	U3	74VHC1G08	
67	1	U4	NUC501BD	
68	1	U6	W25X40L	
69	1	U7	RT9164A-3.3v	

32-BIT ARM7TDMI-BASED MCU

70	1	U8	24LC64
71	1	U9	SP3232ECN
72	1	X1	12MHz
73	1	X2	32.768KHz

32-BIT ARM7TDMI-BASED MCU

NUC501DN CPU Board BOM List:

NUC501AD Revised: Friday, March 13, 2009 Revision: A
 Bill Of Materials March 13,2009 10:57:24 Page1
 Item Quantity Reference Part

1	4	CC1,CC2,CC16,CC17	C/C,1uF
2	9	CC3,CC6,CC7,CC10,CC11,CC12,CC13,CC14,CC15	C/C,0.1uF
3	4	CC4,CC5,CC8,CC9	C/C,20pF
4	1	CT1	T/C,47uF/10V
5	2	JR1,JR2	CONN RECT 15x2
6	1	L1	FB
7	1	R1	22
8	1	R2	10M
9	12	R3,R4,R5,R6,R7,R8,R9,R10,R11,R12,R13,R14	4.7K
10	1	U1	NUC501AD
11	1	U2	W25X40
12	1	U3	XC6206p
13	1	X1	12MHz
14	1	X2	32.768KHz

32-BIT ARM7TDMI-BASED MCU

VPP supplier Board BOM List:

NUC501/VPP Supplier Revised: Tuesday, March 03, 2009 Revision: A

Bill Of Materials March 3,2009 15:49:08 Page1

Item	Quantity	Reference	Part
1	2	CC6,CC1	C/C,10uF
2	2	CC2,CC4	C/C,4.7uF
3	2	CC5,CC3	C/C,1uF
4	1	CC7	C/C,22nF
5	3	D1,D2,D3	MBR0520/RB521S
6	1	L1	6.8uH
7	1	P1	5PX1
8	1	Q1	Si2301ADS
9	1	Q2	Si2302ADS
10	1	Q3	2N3904
11	1	R1	22
12	2	R2,R9	100K
13	1	R2	TBD
14	3	R3,R6,R8	10K
15	1	R4	1.5K
16	1	R7	330
17	1	U1	PC113/AIC1648
18	1	U2	RT9193-1.8v

32-BIT ARM7TDMI-BASED MCU

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